REMARKS

Claims 1-30 and 32-34 are pending in the application. The Applicants' attorney has amended claims 1-5, 8-10, 20-25, 27-28, 30, and 32-33, has cancelled claim 31 without prejudice or disclaimer, and has added new claim 34.

In a teleconference on November 10, 2005, the Examiner stated that she would consider allowing the claims if amended as discussed during the teleconference even though a notice of appeal has been filed. Therefore, the Applicant's attorney requests that after reviewing this amendment, the Examiner contact him to inform him of her decision so that he can take the appropriate action.

In view of the following, all previously unallowed claims are in condition for allowance.

Rejection of Claims 1-33 Under 35 U.S.C.103(a) As Being Unpatentable Over Patapoutian In View of Fredrickson et al. ("Fredrickson")

Claim 1

Claim 1 as amended recites a coded binary sequence including a first group of consecutive bits having first and second separate portions and representing a first logic level, the bits in the first portion each having a first state and the bits in the second portion each having a second state, and a second group of consecutive bits each having a same state, the second group representing a second logic level.

For example, referring to paragraph 25 and FIG. 5 of the present application, a coded binary sequence includes a first code symbol (50a and 50b) that has a first group of consecutive bits 0011 having first (00) and second (11) portions and representing a first logic level (logic 1), the bits in the first portion each having a first state (logic 0) and the bits in the second portion each having a second state (logic 1). The coded binary sequence also includes a second code symbol (50e and 50f) that has a second group of consecutive bits 0000 each having a same state (logic 0).

Patapoutian, on the other hand, fails to disclose a group of consecutive bits each having a same state and representing a logic level. Referring to, *e.g.*, col. 3, Lines 55-58, although Patapoutian codes a binary one information value (logic level "1") as a group "--++" of consecutive bits and codes a binary zero information value (logic level "0") as a group "++--" of consecutive bits, neither of these groups ("--++" and "++--") includes bits each having the same state. In other words, to read on claim 1, at least one of Patapoutian's groups would have to include bits having the same state (*e.g.,*"----" or "++++").

Moreover, Fredrickson fails to disclose or suggest the teaching missing from Patapoutian, namely a group of consecutive bits each having the same state, the group representing a logic level.

Claims 2-30 and 32-34

These claims are patentable for reasons similar to those recited above in support of the patentability of claim 1.

CONCLUSION

In view of the foregoing, all claims are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes that a telephone conference would expedite prosecution of this application, please telephone the undersigned at 425.455.5575. If the Examiner does not agree that all claims are in condition for allowance, the Examiner is respectfully requested to telephone the undersigned prior to issuing an advisory action in this case.

In the event additional fees are due as a result of this amendment, you are hereby authorized to charge such payment to Deposit Account No. 07-1897.

Respectfully submitted,

Dated: December 6, 2005

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